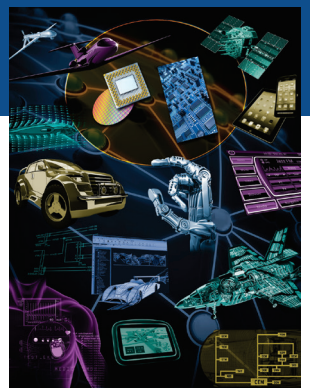
N10/N7 Demand an Innovative Approach to SRAM IP Verification for Improved Manufacturability

Mentor, a Siemens Business / MediaTek

ABSTRACT

For any new node, static random-access memory (SRAM) is a foundational element of the intellectual property (IP) provided by foundries. Because SRAM is constructed using features at the “edge” of a new node’s process capabilities, ensuring SRAM manufacturability is crucial to the success of IP used in process development and process characterization. The best means of ensuring high quality designs is to use the SRAM IP as characterized during process development, but the complexity of SRAM makes verification extremely challenging. Mentor collaborated with TSMC to develop an innovative SRAM IP verification methodology, using a flow that integrates Calibre Pattern Matching and Calibre nmDRC functionality to provide an unprecedented level of accuracy that ensures the implemented SRAM matches the SRAM that was validated during process development. Previously, with no means to validate that the SRAM was DRC-clean, fabless customers were unaware that non-recommended SRAM modifications might remain in design tapeouts. Utilizing the Calibre Pattern Matching approach, TSMC can now fully describe the SRAM checks to ensure SRAM is implemented as intended. MediaTek, as a fabless customer of TSMC, not only achieved fast sign off verification, but also acquired a richer, more comprehensive understanding of the foundry’s SRAM requirements. The pattern-based flow is capable of securing all SRAM IP by checking far more than previous SRAM verification methodologies, including design rule coverage of all inter-cell, intra-cell, intra-layer, and between SRAM blocks requirements. In this presentation, you will learn about the challenges of SRAM verification, the new verification methodology developed by TSMC and Mentor, and MediaTek’s experience and results with this innovative technology.



TSMC OIP 2017:
N10/N7 Demand an Innovative Approach to SRAM IP Verification for Improved Manufacturability

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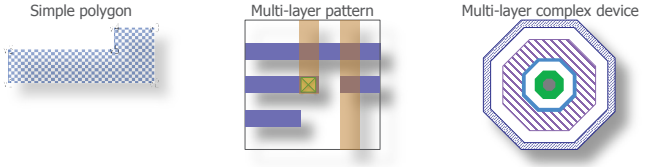
A Tool to Search Any Geometries

- Pattern Matching is a tool for locating specific geometries in any design layout
  - No size restriction
  - Visualize search patterns
  - Clear communication via patterns
- From simple to the most complex geometric configurations

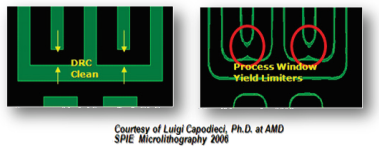
Simple polygon | Multi-layer pattern | Multi-layer complex device



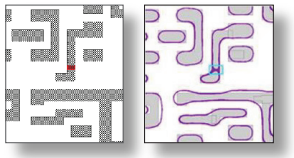
- Integration with DRC enables powerful design verification flows

Expanding Applications for Patterns

- Pattern Matching's original niche: complementing rule-based definitions to find hotspot patterns



Courtesy of Luigi Capodieci, Ph.D. at AMD SPIE Microlithography 2006

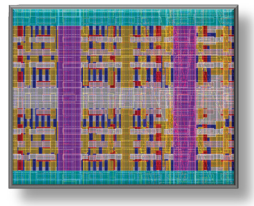


Simulation detected pinch

- General pattern match capabilities
  - Easily handles multiple geometry, multiple layers
  - Exact geometry matching or fuzzy/variability constraint
  - Orientation-aware processing

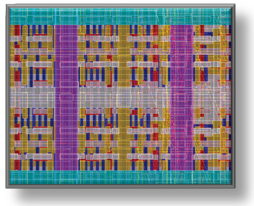
Application Growth of Pattern Matching

- The past several years have seen major growth in the applications of pattern matching, both for foundry and fabless flows
  - Layout enhancement
  - Orientation & symmetry checking
  - Layout analysis
  - Device matching (ex. diode, inductor)
  - **SRAM verification**



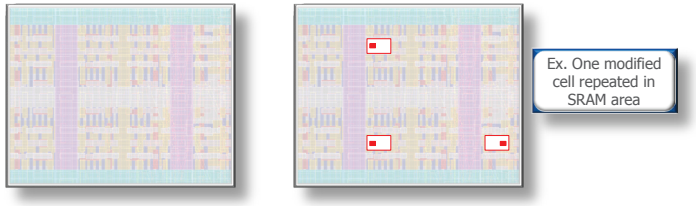
Designed to the Tightest Margins

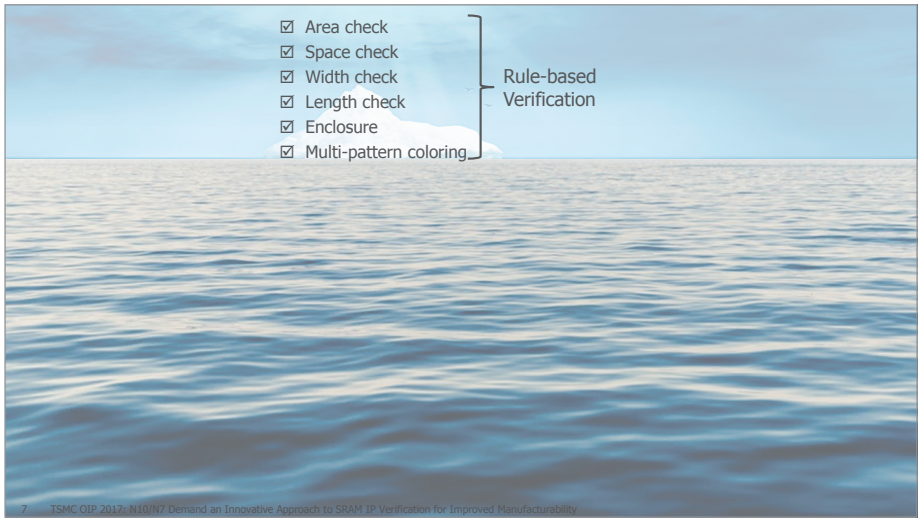
- SRAM libraries provided by foundries are certified and any changes can have drastic impacts to functionality and manufacturability
- SRAMs are usually designed to the minimum process margin
- For ≤16nm, the engineering time required to resolve any issue is very costly
- Using SRAM libraries as they were qualified during process development ensures optimal manufacturability

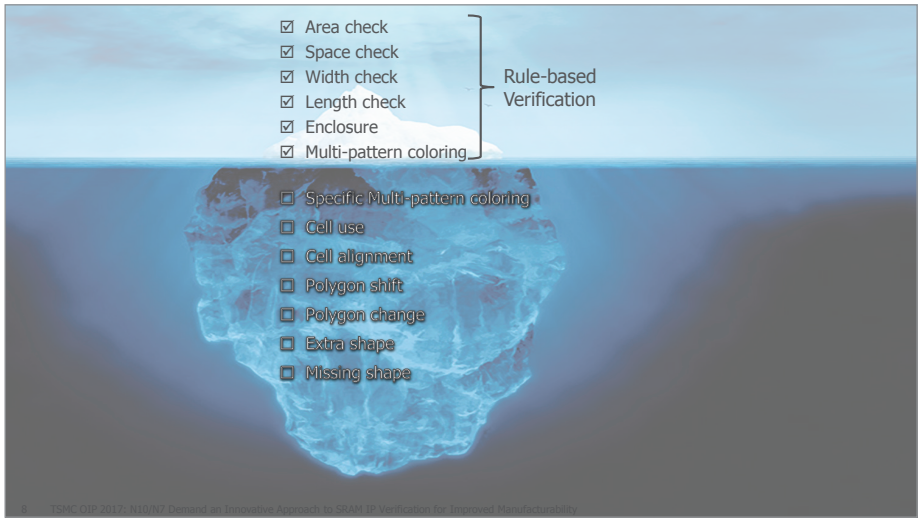


Modifications to SRAM IP

- Changes occur at every node, whether intentionally or not
- Nearly all designs have modifications in the SRAM area

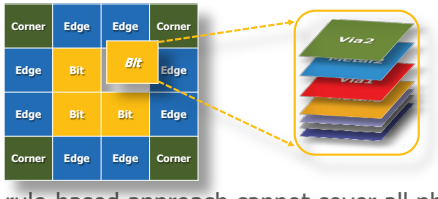






Source of Challenge

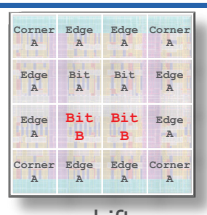
- SRAM blocks consist of multiple cells and each cell includes many layers



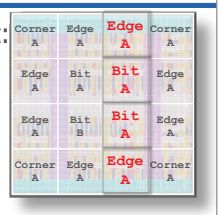
- Traditional rule-based approach cannot cover all physical errors across cell, layer, and blocks
- Cell-based approach cannot cover library cell swapping, alignment, or hierarchy errors

The Challenge to Manufacturing Teams

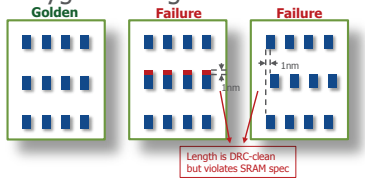
- Cell misuse:



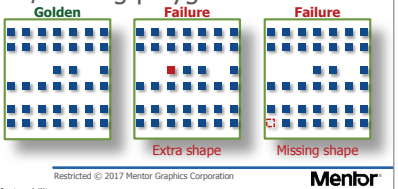
- Cell misalignment:



- Polygon change or shift:

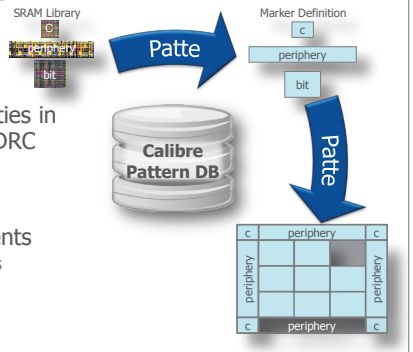


- Extra/Missing polygons:



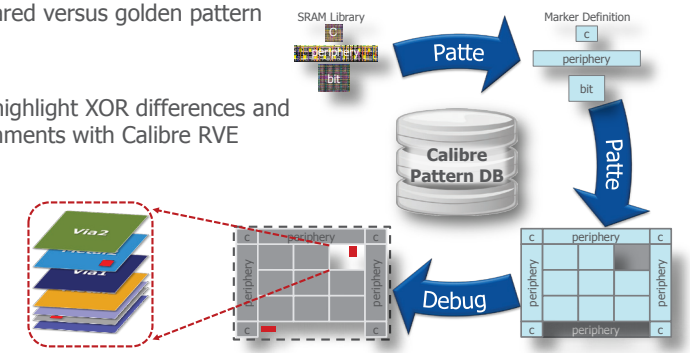
Building the Right Solution: PM-Based Verification

- TSMC/Mentor collaborated on an innovative SRAM IP verification methodology
- Built utilizing the pattern matching capabilities in Calibre PM and integrated with Calibre nmDRC
- Full coverage of foundry's SRAM requirements
  - Inter-cell, intra-cell, and intra-layer design rules
  - Simultaneously handling multiple block types



PM-Based SRAM Verification and Error Identification

- Error identification: Patterns matched per cell and compared versus golden pattern
- Visualization: highlight XOR differences and rule check comments with Calibre RVE



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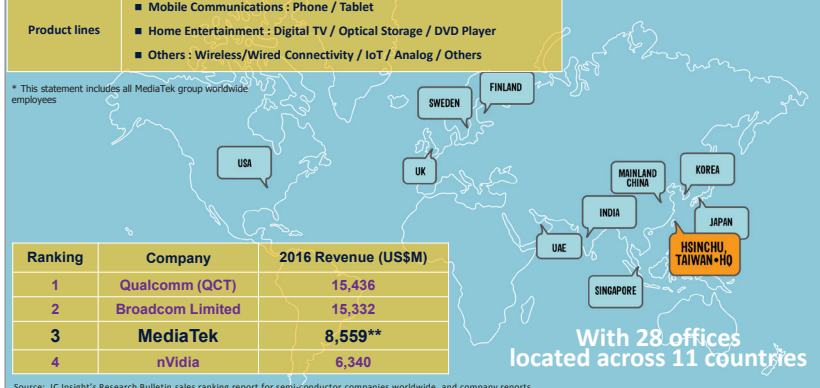
Who we are

Headquarters	Science Park, Hsinchu, Taiwan
Employees	More than 15,000 employees worldwide across 28 offices*
Product lines	■ Mobile Communications : Phone / Tablet ■ Home Entertainment : Digital TV / Optical Storage / DVD Player ■ Others : Wireless/Wired Connectivity / IoT / Analog / Others

* This statement includes all MediaTek group worldwide employees



With 28 offices located across 11 countries

Ranking	Company	2016 Revenue (US$M)
1	Qualcomm (QCT)	15,436
2	Broadcom Limited	15,332
3	MediaTek	8,559**
4	nVidia	6,340

Source: IC Insight's Research Bulletin sales ranking report for semi-conductor companies worldwide, and company reports
** Revenue calculation is MediaTek's official revenue of 2016 varies slightly from IC Insight's report, but it has no impact to its ranking position on the report.

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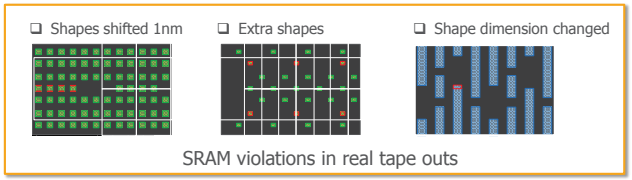
MediaTek Real Use Case

- TSMC requires SRAM clean for N10 and below
  - SRAM modifications = potential manufacturing risk
  - Conventional verification and debugging practices require ~2 weeks to resolve through back and forth communication per error
- Using TSMC's SRAM checker, MediaTek could verify SRAM macros are clean and prevent real errors prior to tape out



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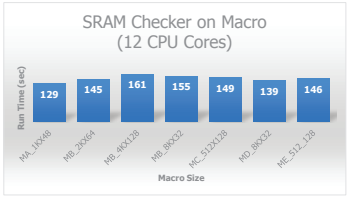
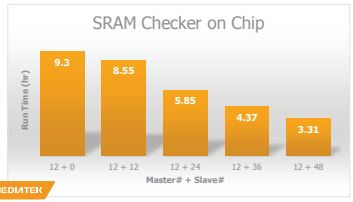
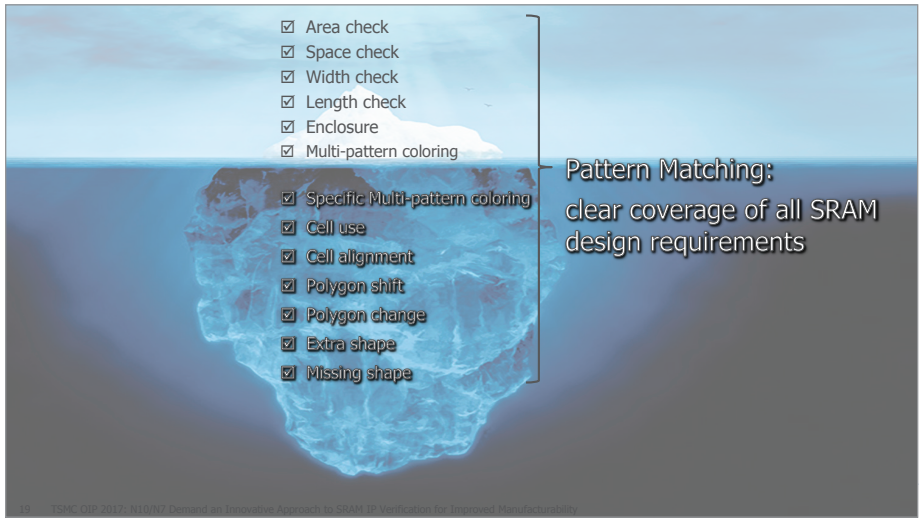
New Flow Experience





- Simple Usage
  - Same as DRC
  - "calibre –drc –hier –turbo …"
- Excellent performance
  - It takes 2 to 3 minutes to check one memory macro.
  - It shows good scalability to run with multiple machines.
- It provides full coverage checks and eliminates the iterations with TSMC to revise SRAM macros.

SUMMARY



Summary

- TSMC partnered with Mentor to build SRAM verification checks with 100% coverage
  - Assurance all SRAM blocks have no designer-induced process impacts
  - Calibre reports problematic cells and exact locations of errors
- Flow is proven at both fabless and foundry sides
- Fabless customers achieve fast sign off verification with a richer understanding of the TSMC's SRAM requirements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